CLAIMS

1. Delay fault test circuitry for producing a train of two clock pulses in response to two respective clock signals of different frequency associated with logic circuits arranged to run at different speeds, and arranged such that the rising edges of the second of the clock pulses are aligned, the circuitry including:

counting means for producing a reference count value;

means for initiating the first of the two clock pulses when the said count value reaches a first threshold value;

means for ending the first of the two clock pulses when the said count value reaches a second threshold value;

means for initiating the second of the two clock pulses when the said count value reaches a third threshold value;

means for ending the second of the two clock pulses when the count value reaches a fourth threshold value; wherein

the third threshold value is common for both input clock signals and the first, second and fourth threshold values are based on the respective frequencies of the clock signals.

2. Delay fault test circuitry as claimed in Claim 1, wherein the said first, second and fourth threshold values comprise functions of the ratio of the fastest clock frequency to the clock frequency associated with the logic circuitry under test.

3. Delay fault test circuitry as clamed in Claim 2, wherein the first, second and fourth threshold values are functions of the maximum of the aforesaid ratios.

4. Delay fault test circuitry as claimed in Claim 3, wherein the first threshold value is derived from the difference between the said maximum ratio

value and the ratio value for the clock signal associated with the logic circuit under test

5. Delay fault test circuitry as claimed in Claim 3 and 4, wherein the second threshold value is determined on the basis of the difference between the said maximum ratio value and half of the ratio value for the clock signal associated with the logic circuit under test, if the said ratio value comprises an even number.

6. Delay fault test circuitry as claimed in Claim 3 and 4, wherein the second threshold value is determined on the basis of the difference between the maximum ratio value and half of the ratio value for the clock signal associated with the logic circuit under test, plus one, if the particular ratio comprises an odd number.

7. Delay fault test circuitry as claimed in any one or more of Claims 4, 5 or 6, wherein the fourth threshold count value is determined on the basis of the sum of the maximum ratio and half of the particular division ratio of the clock signal associated with the logic circuit under test.

8. Delay fault test circuitry as claimed in any one or more of the preceding claims, and including a ratio generator in which the aforementioned ratio is implemented by way of a counter.

9. Delay fault test circuitry as claimed in Claim 8 and employing two counters in order to calculate each of the aforesaid ratios.

10. Delay fault test circuitry as claimed in Claim 9, wherein the first of the two counters is arranged to be fed by the fastclk signal and arranged to receive an enable signal generated by the other of the two said counters.

11. Delay fault test circuitry as claimed in Claim 10, wherein the second counter is arranged to be fed by the clock signal with respect to which the division ratio is to be calculated.

12. Delay fault test circuitry as claimed in Claim 11, wherein the least significant bit of the said second counter comprises the enable signal delivered to the said first counter, and wherein the most significant bit of the second counter comprises a signal indicating that the required ratio has been determined.

13. Delay fault test circuitry as claimed in any one or more of Claims 3 to 7, and including a fastclk pulse generator in which an enable signal is generated within a window defined by reference to the said maximum ratio.

14. A method of producing a delay fault test signal comprising a train of two clock pulses in response to two respective clock signals of different frequency associated with logic circuits arranged to run at different speeds, and wherein the rising edges of the second of the clock pulses are aligned, the method including the steps of:

producing the reference count value;

initiating a first of the two clock pulses when the said count value reaches a first threshold value;

ending the first of the two clock pulses when the said count value reaches a second threshold value;

initiating the second of the two clock pulses when the said count value reaches a third threshold value;

ending the second of the two clock pulses when the count value reaches a fourth threshold value; wherein

the third threshold value is common for both input clock signals and the first, second and fourth threshold values are based on the respective frequencies of the clock signals.

15. A method of producing a delay fault test signal as defined in Claim 14 and including steps conducted in accordance with the circuitry of any one or more of Claims 2 to 13.